Introducing the UCIe™ 2.0 Specification: Supporting 3D Packaging and Manageability System Architecture

Dr. Debendra Das Sharma
Intel Senior Fellow and co-GM Memory and I/O Technologies, Intel Corporation
Chair of UCIe Consortium

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

Meet the Presenter

Dr. Debendra Das Sharma

Intel Senior Fellow and co-GM Memory and I/O Technologies, Intel Corporation

UCIe Consortium Chairman

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

Agenda

- Introducing UCIe
- UCIe 1.0/1.1: Overview
- UCIe 2.0: Vertical Chiplets with UCIe-3D
- UCIe 2.0: Addressing SIP challenges through common infrastructure
- Future Directions and Conclusions

UCIe™
Universal Chiplet Interconnect Express

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

Universal Chiplet Interconnect Express™ (UCIe):

An Open Standard for Chiplets

Guiding principles of UCIe

1. Open Ecosystem with Plug-and-play
2. Backward compatible evolution when appropriate to ensure investment protection
3. Best power, performance, and cost metrics across the industry applicable across the entire compute continuum
4. Continuously innovate to meet the needs of evolving compute landscape

(Leveraging decades of experience driving successful industry standards at the board level: PCIe, CXL, USB, etc.)

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

Board Members

Leaders in semiconductors, packaging, IP suppliers, foundries, and cloud service providers are joining together to drive
The open chiplet ecosystem.

JOIN US!

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

130+ Member Companies…and growing!

Achronix Semiconductor Corp
Advanced Micro Devices
Advanced Semiconductor Engineering, Inc.
Advantest America, Inc.
Akrostar Technology Co., Ltd
Alchip Technologies, Ltd. Taiwan Branch
Alibaba Inc.
Alphawave Semi
Amkor Technology, Inc.
Ampere Computing
Analog Devices Incorporated
AP Memory Technology Corporation
Applied Materials, Inc.
Arm Limited
Arteris, Inc.
ASMedia Technology Inc.
Astera Labs
Atron (Chongqing) Technologies, Limited
Ayar Labs
Beijing Henghuizhixun Technology Co., Ltd.
Blue Cheetah Analog Design Inc.
BMW of North America LLC
Broadcom Inc.
Cadence Design Systems Inc.

Ceremorphic, Inc.
ChangXin Memory Technologies, Inc.
Ciena Corporation
CoMira Solutions Inc
Credo Semiconductor, Inc
Deca Technologies, Inc.
DENSO Corporation
d-Matrix
Douyin Vision Co., Ltd
Dream Chip Technologies GmbH
DreamBig Semiconductor Inc.
ECARX Limited
Egis Technology Inc.
e-Infochips Inc (An Arrow Company)
Eliyan Corp.
Ericsson AB
eTopus Technology Inc.
EVAS Intelligence Co., Ltd.
EXTOLL GmbH
ForwardEdge ASIC
FuriosaAi
Futurewei Technologies, Inc.
Global Unichip Corporation (GUC)
GlobalFoundries U.S. Inc.
GM Global Technology Operations LLC

Google
HANA Micron, Inc.
Honda Motor Co., Ltd.
Huixi Technology Co. Ltd (Rhino Auto)
IBM
Imec vzw
Infineon Technologies AG
InfiniLink Inc.
Innosilicon Microelectronics (Wuhan) Co. LTD.
Inpsytech,Inc.
Intel Corporation
JCET Group Co., Ltd.
Kandou Bus SA
Keysight Technologies
Kiwimoore (Shanghai) Semiconductor Co., Ltd_
KNiulink Semiconductor Ltd.
Kyocera-AVX
LG Electronics
Lightmatter
M SQUARE Ltd. Shanghai
M2 Semiconductor Ltd.
Macronix International Co., Ltd
Marvell Asia PTE Ltd
MediaTek Inc.
Mercedes-Benz Research & Development North America, Inc.

Meta Platforms, Inc.
Microchip Technology Inc.
Micron Technology Inc
Microsoft
MIPS Tech LLC
MIRISE Technologies Corporation
Mixel, Inc.
MosChip Technologies
National Institute of Advanced Industrial Science and Technology
nepes Corporation
Neuchips Inc.
Neuron IP Inc
NHanced Semiconductors, Inc.
Nippon Telegraph and Telephone Corporation
Nissan Motor Co., Ltd.
Nokia Solutions and Networks Oy
Nuclei System Technology Co., Ltd
NVIDIA
OPENEDGES Technology. Inc.
Physim Electronics Technology Co., LTD
Powerchip Semiconductor Manufacturing Corp (PSMC)
proteanTecs, LTD.
Qualcomm, Inc.
Qualitas Semiconductor
Rapidus Corporation

Rebellions
Renesas Electronics Corporation
Robert Bosch GmbH
Rohde & Schwarz GmbH & Co. KG
Samsung Electronics Co, Ltd.
Sanechips Technology Co., LTD
Semitronix Corporation
Shanghai UniVista Industrial Software Group Co., Ltd.
Shanghai Zhaoxin Semiconductor Co., Ltd.
Shinko Electric Industries Co., LTD.
Siemens Industry Software Inc.
SiliconAuto B.V.
Siliconware Precision Industries Co. Ltd.
SK Hynix Inc.
SkyeChip
SmartDV Technologies
Socionext Inc.
Synopsys Inc
Taiwan Semiconductor Manufacturing Co., Ltd.
Tektronix Inc
Tenstorrent Inc.
Teradyne, inc.
Texas Institute for Electronics, The University of Texas at Austin
Texas Instruments Incorporated
The MathWorks, Inc.

Thine Electronics, Inc.
Tongfu Microelectronics Co., Ltd
Toyota Motor Corporation
Truechip Solutions PVT LTD
Tsavorite Scalable Intelligence, Inc
Unisoc (Shanghai) Technologies Co., Ltd
University of New Hampshire
Untether AI
Valens Semiconductor
Ventana Micro Systems Inc
VeriSilicon, Inc.
VIA NEXT Technologies, Inc.
Volkswagen Aktiengesellschaft
Winbond Electronics Corporation
xFusion Digital Technologies Co., Ltd
Xi'an UniIC Semiconductors Co.,Ltd.
Xpeedic Co., Ltd.
Xsight Labs Ltd.
Zero ASIC Corporation
Zhejiang Zentel Memory Technology Co., Ltd.

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

UCIe Consortium is Open for Membership

- UCIe Consortium welcomes interested companies and institutions to join the organization at the **Contributor and Adopter level.**

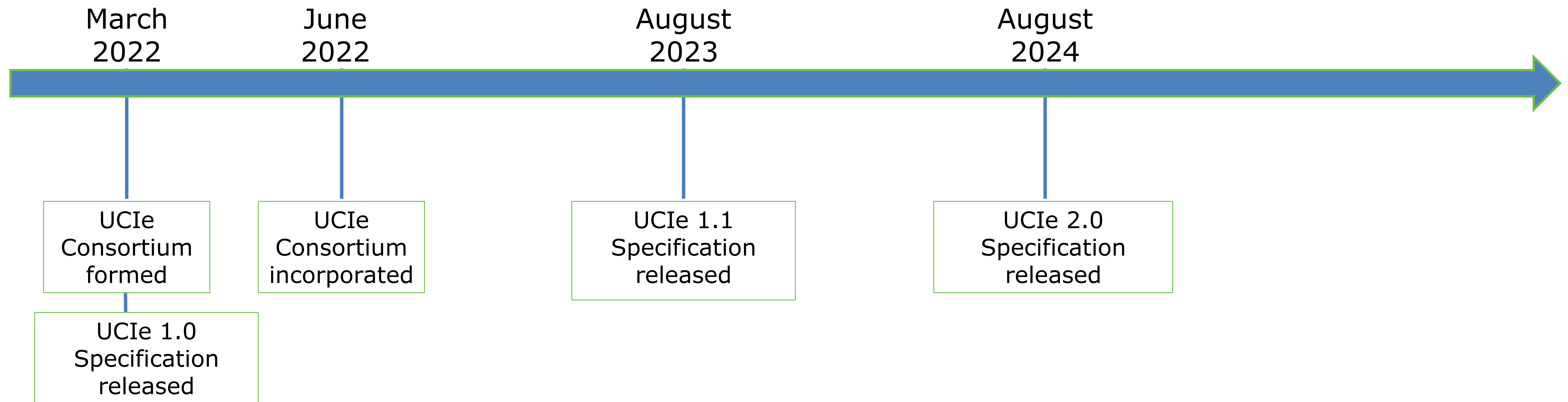
- **UCIe** was founded in March 2022, incorporated in June 2022. Two levels of memberships: Contributor and Adopter

- **Contributor Membership**
  - Access the Final Specifications (ex: 1.0, 1.1, 2.0, etc.)
  - Implement with the IP protections as outlined in the Agreements
  - Right to attend Corporation trade shows or other industry events as determined by the Board
  - Participate in the technical working groups
  - Influence the direction of the technology
  - Access the intermediate (dot level) specifications
  - Election to get to the Promoter Class/ Board every year when the term of half the board completes

- **Adopter Membership**
  - Access the Final Specifications (ex: 1.0, 1.1, 2.0, etc.), but not intermediate level specifications
  - Implement with the IP protections as outlined in the Agreements
  - Right to attend Corporation trade shows or other industry events as determined by the Board

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

Member Driven Evolution

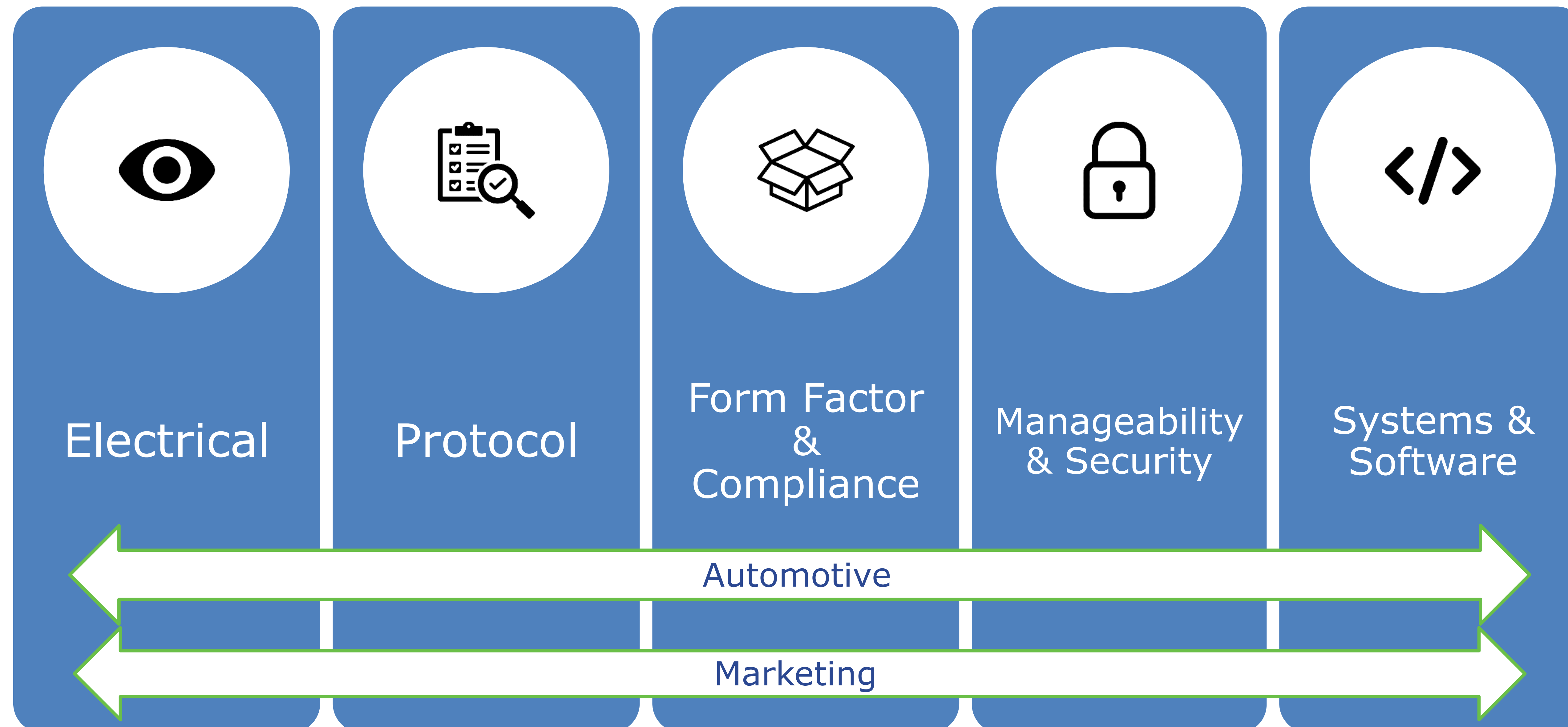


UCIe™ Universal Chiplet Interconnect Express

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

UCIe Consortium Working Groups

Working Groups are identifying and addressing the demands of a complete, full-stack solution for strengthening the open standards-based ecosystem.



UCIe™
Universal Chiplet Interconnect Express

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

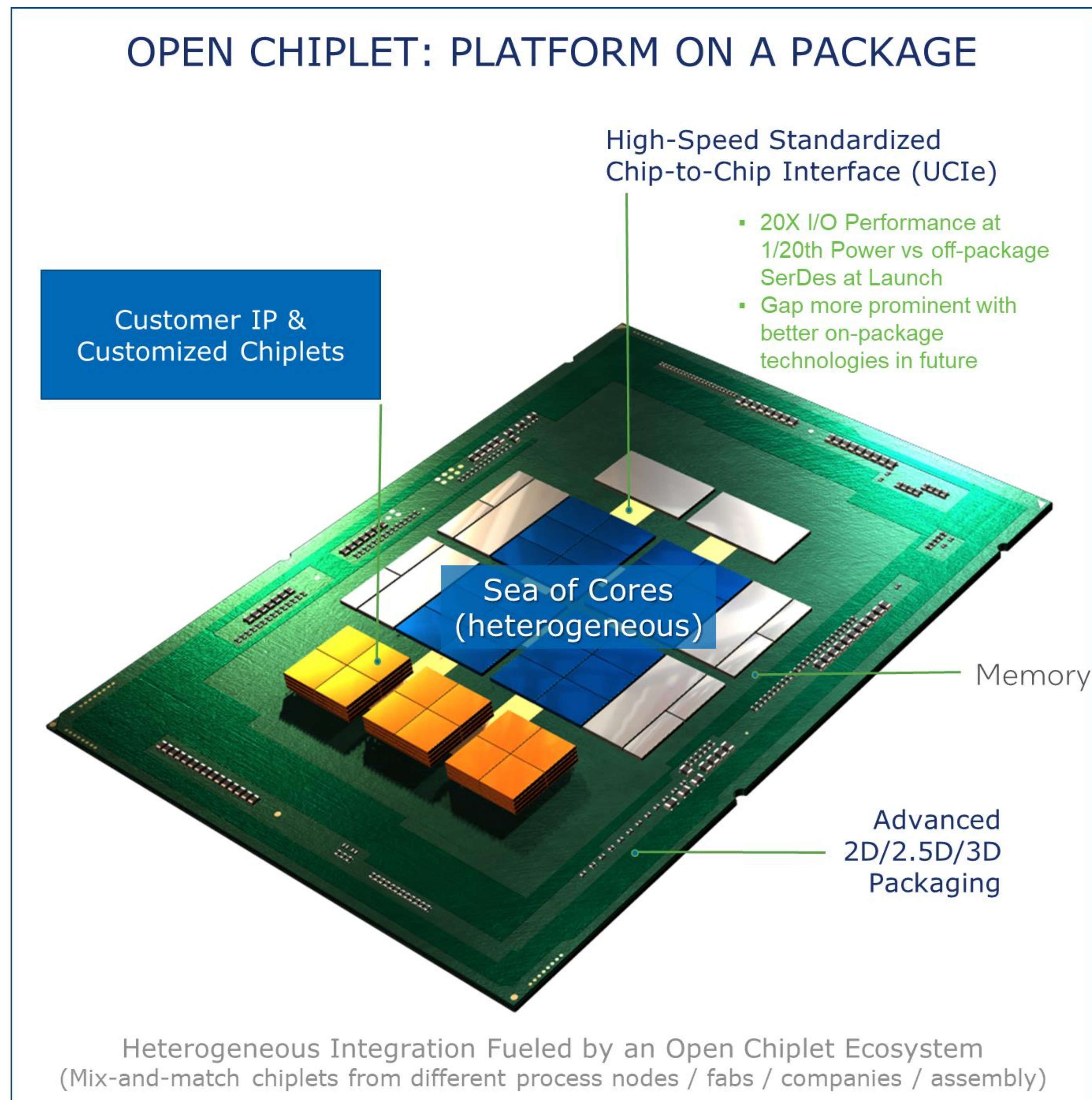
Agenda

- Introducing UCIe
- UCIe 1.0/1.1: Overview
- UCIe 2.0: Vertical Chiplets with UCIe-3D
- UCIe 2.0: Addressing SIP challenges through common infrastructure
- UCIe – Key Metrics
- Future Directions and Conclusions

UCIe™
Universal Chiplet Interconnect Express

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

Motivation for UCIe



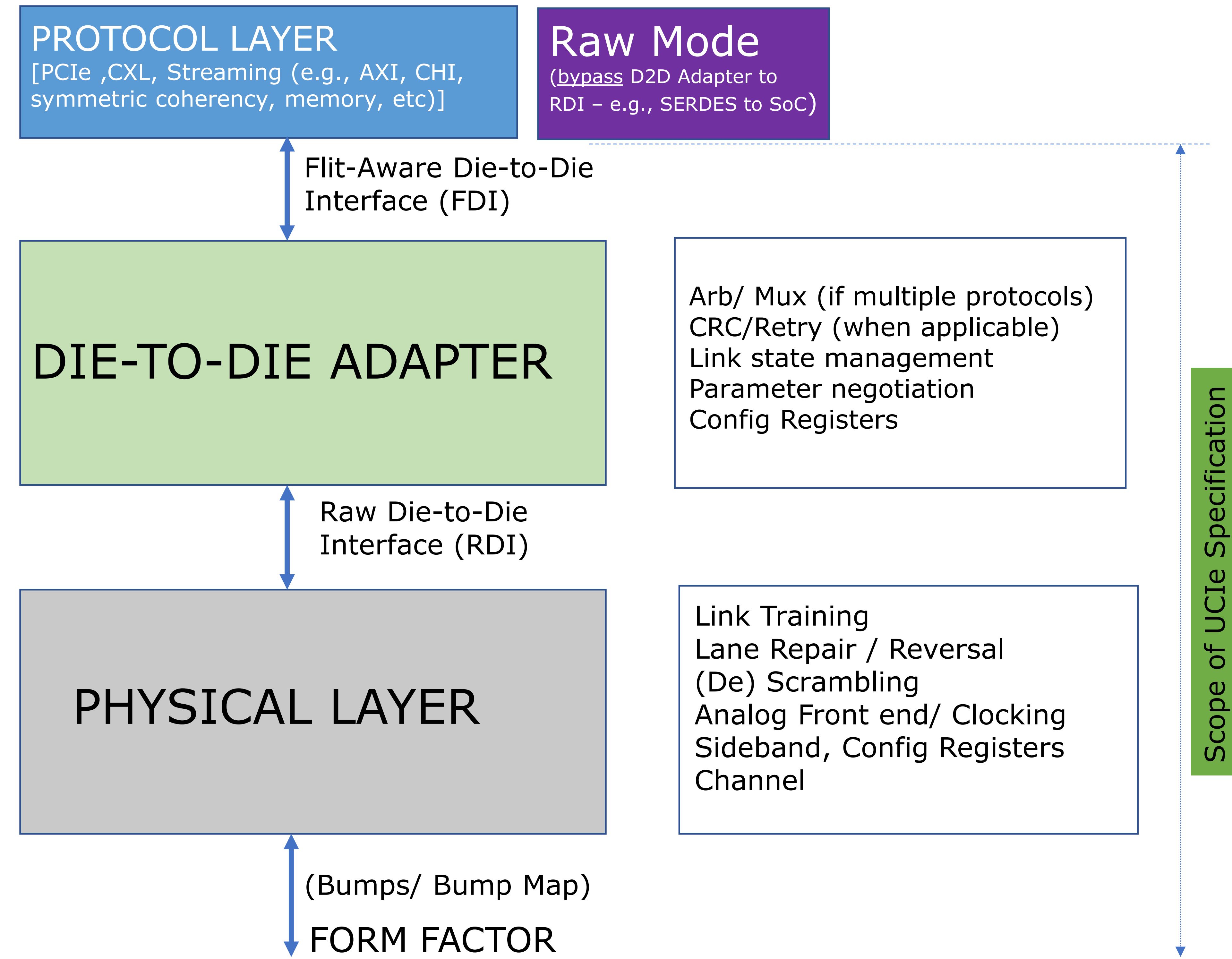
- Overcome reticle limits – SoC is now at package level
- Reduces time-to-solution (e.g., enables die reuse)
- Lowers portfolio cost (product & project)
  - Optimal process
  - Smaller dies => better yield
  - Reduces IP porting costs
  - Lowers product SKU cost
- Bespoke solution
  - Mix-and-match with a standard interface
- Scales innovation (Mfg. process locked IPs)

UCIe driving Industry alignment! Package is the new platform!

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

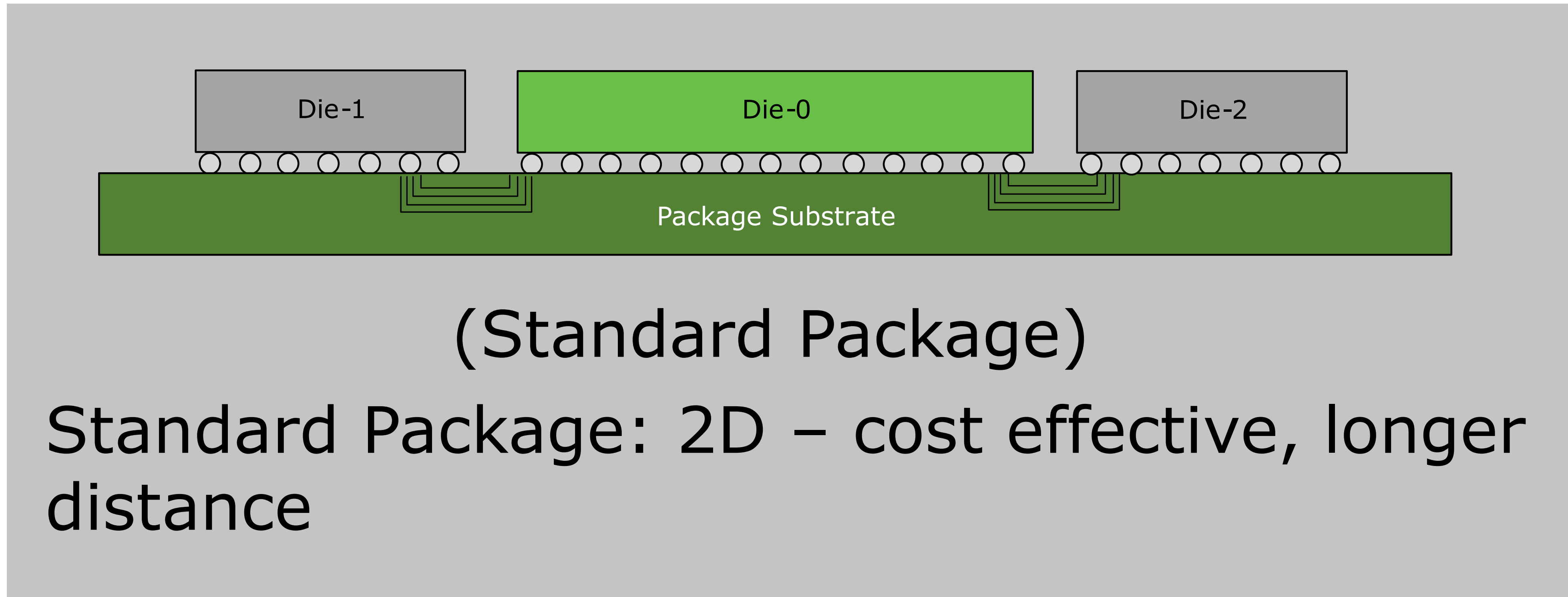
UCIe 1.0 and 1.1 Specification: 2D/ 2.5D interconnect

- **Layered Approach - industry-leading KPIs**
- **Physical Layer:** Die-to-Die I/O
- **Die to Die Adapter:**
  - Reliable delivery, Multi-protocol support
- **Protocol:**
  - **CXL®/PCIe® for volume attach, plug-n-play**
    - SoC construction issues are addressed w/ CXL/PCIe
    - Usages: I/O attach, Memory, Accelerator
  - **Streaming for other protocols**
    - Scale-up (e.g., CPU/ GP-GPU/Switch from smaller dies)
- **Well defined specification**
  - Configuration register for discovery and run-time
  - Form-factor and Management
  - Compliance for interoperability
  - Plug-and-play IPs with RDI/ FDI interface



Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

UCIe 1.0/1.1 : Supports Standard and Advanced Packages

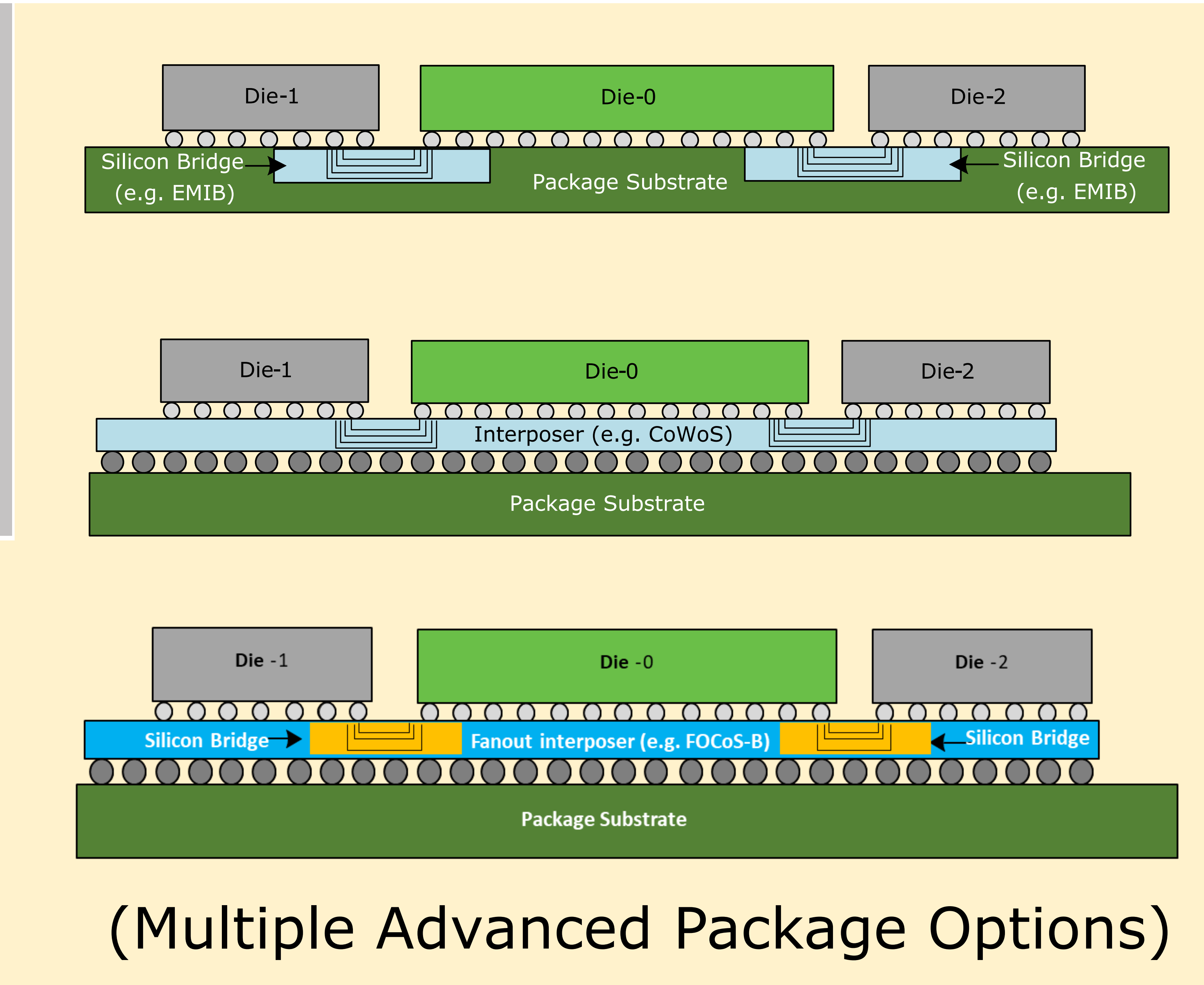


(Standard Package)

Standard Package: 2D – cost effective, longer distance

Advanced Package: 2.5D – power-efficient, high bandwidth density

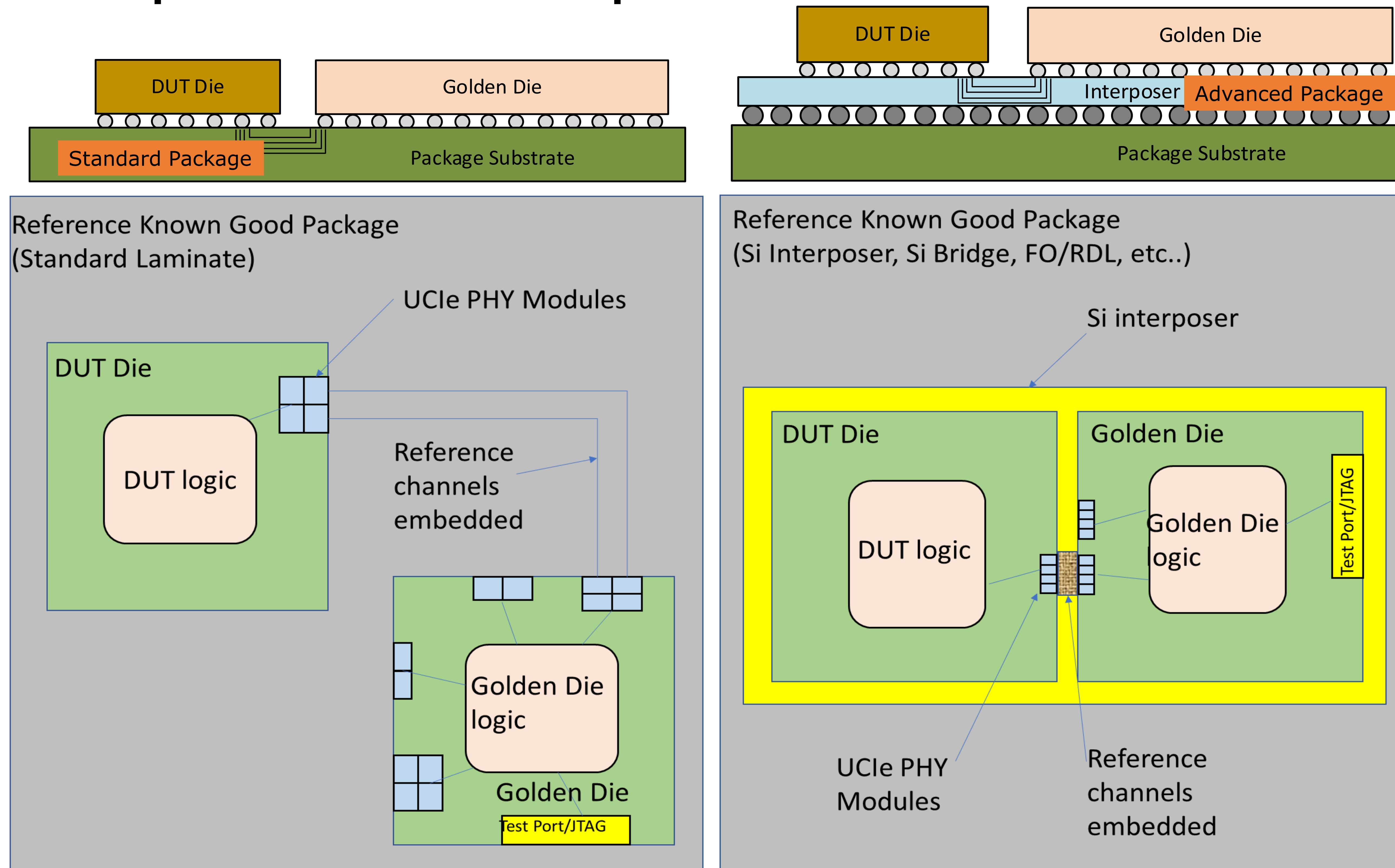
Dies can be manufactured anywhere and assembled anywhere – can mix 2D and 2.5D in same package: Flexibility for SoC designer



(Multiple Advanced Package Options)

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

UCIe Compliance: Setup

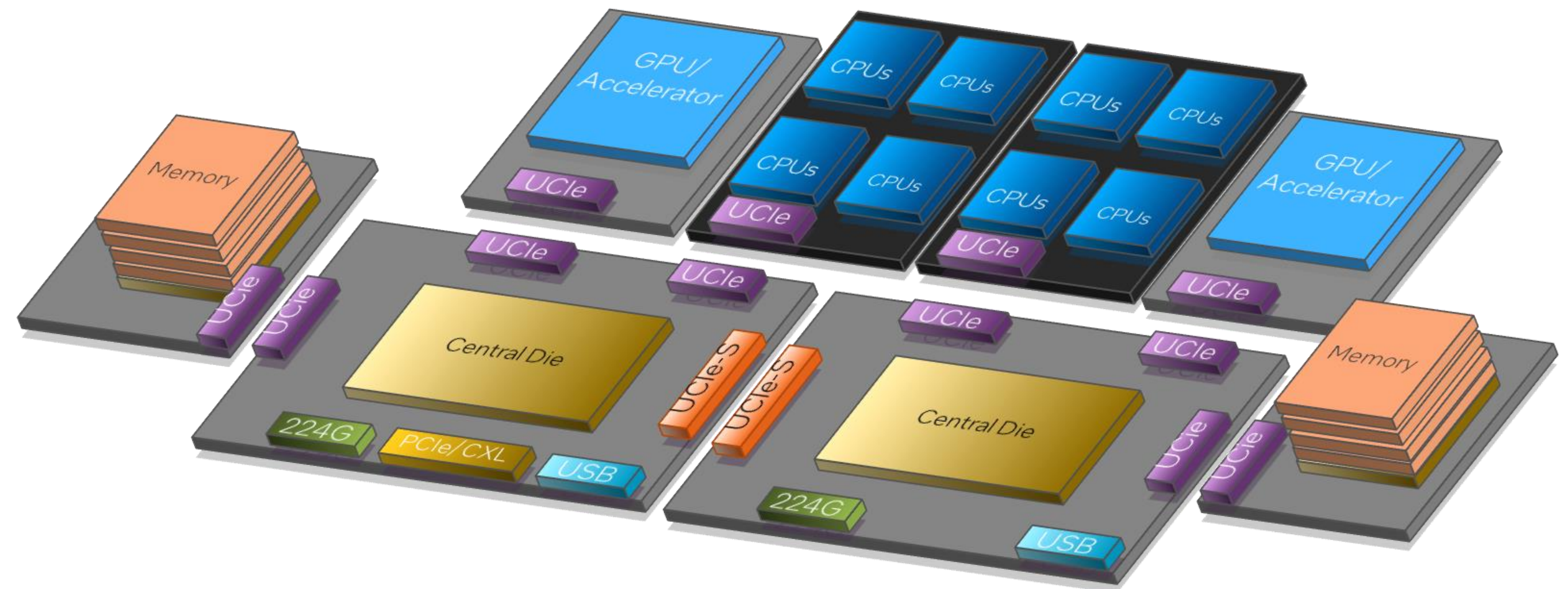


Ingredients: Reference known good package with Reference Channels, Golden Die, DUT

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

UCIe Usage Model: System in Package

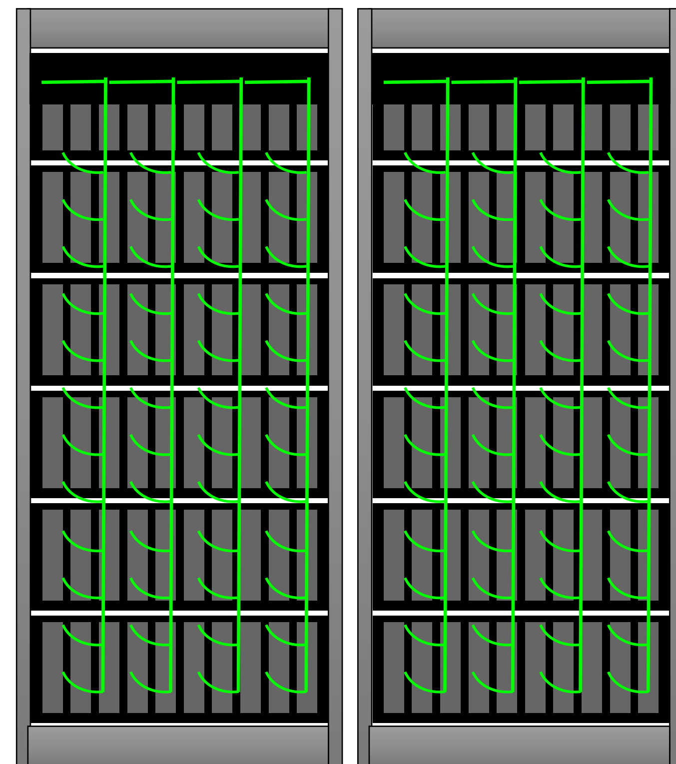
- SoC as a Package level construct
  - Standard and/ or Advanced package
  - Homogeneous/ heterogeneous chiplets
  - Chiplets from multiple suppliers
- Across all segments:
  - Hand-held, Client, Server, Workstation, Automotive, Comms, HPC, etc.
  - Similar to PCIe/ CXL at board level



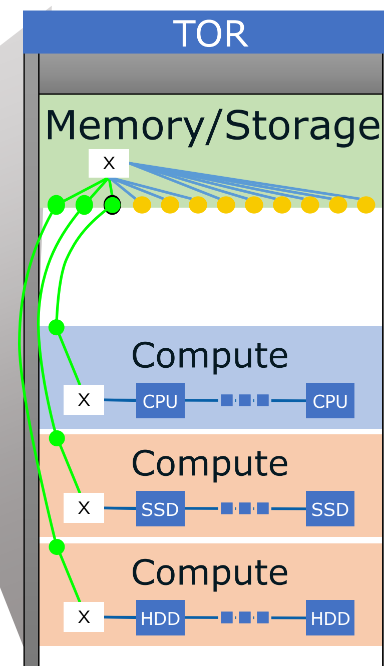
Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

Off-Package Connectivity with UCIe Retimers: Composability at Rack/ Pod Level

Pod of Racks
Physical connectivity
using UCIe-Retimer-based
co-packaged optics
carrying CXL protocol



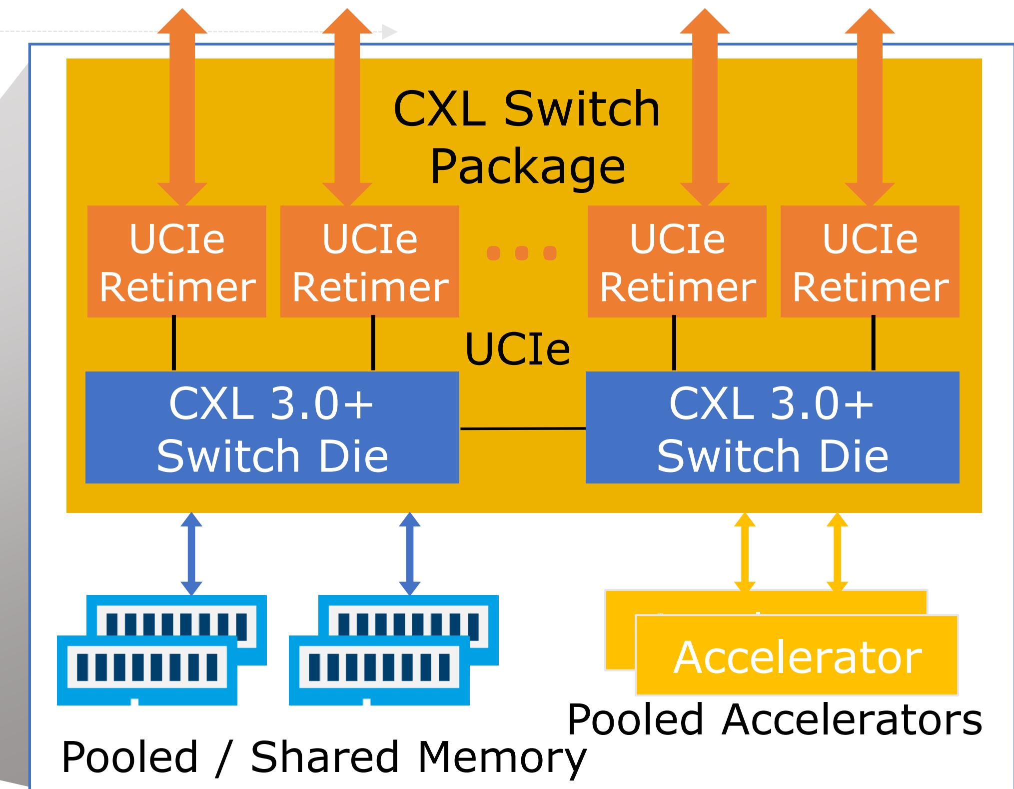
UCIe-based co-packaged Optics
for Rack/Pod Level Connectivity
running CXL protocol

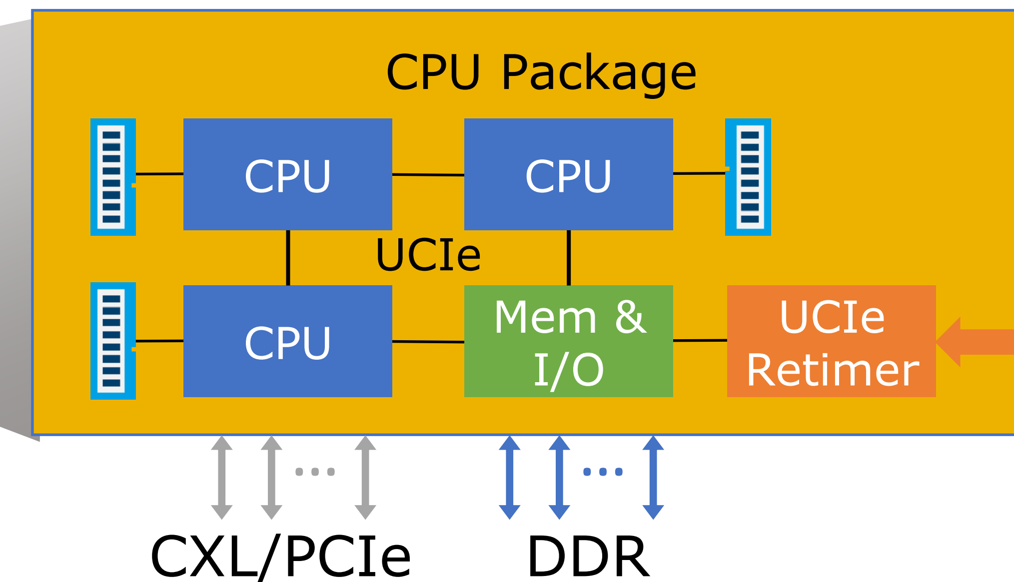


Pooled / Shared
Memory Or
Accelerator Drawer

Compute Drawer

Optical Connection for Intra-Rack and Pod





Optical Connection
to CXL Switch on
Rack

CXL/PCIe DDR
Interconnects at Drawer Level

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

Agenda

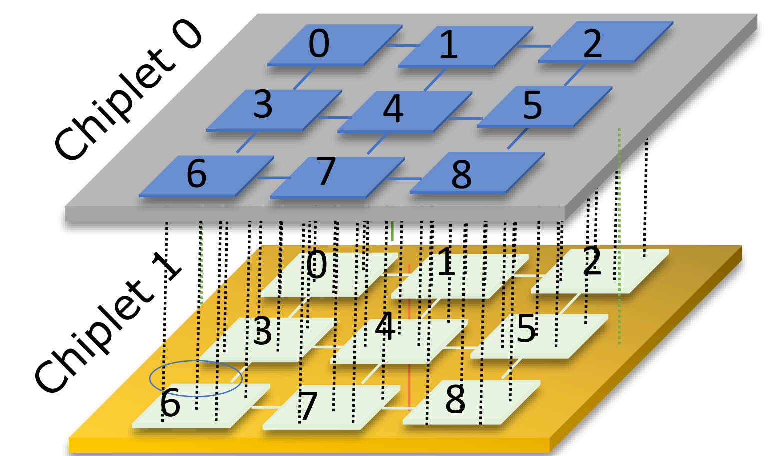
- Introducing UCIe
- UCIe 1.0/1.1: Overview
- UCIe 2.0: Vertical Chiplets with UCIe-3D
- UCIe 2.0: Addressing SIP challenges through common infrastructure
- UCIe – Key Metrics
- Future Directions and Conclusions

UCIe™
Universal Chiplet Interconnect Express

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

UCIe-3D: Opportunities and Challenges

- 3D deployed in commercial offerings (Memory, CPU)
  - Hybrid bonding (HB) looks promising
  - Standardize for constrained interop (e.g., bump pitch match)
- High bandwidth density
  - 3D => areal connectivity (vs shore-line in 2D/ 2.x D)
  - Bump pitches aggressively shrinking
    - Number of wires increases inversely as the square of bump pitch
  - Must ensure we continue to be bump-limited
- Low power
  - Reduced interconnect distance (~0) between dies, electrical parsitics
  - Simple circuits and lower frequency are essential
- Better power, bandwidth, and latency than UCIe 2.5D



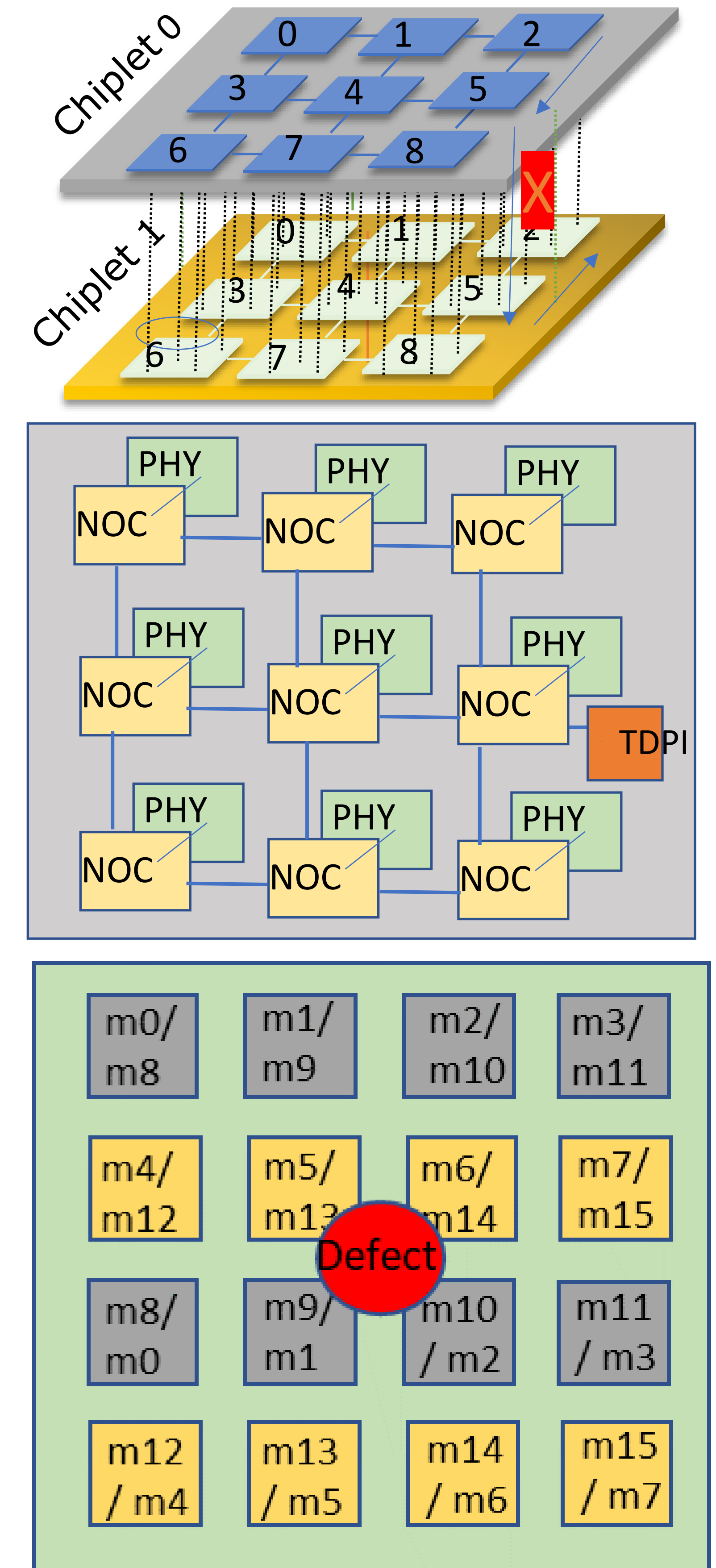
3D can deliver power-efficient performance comparable/ better than large monolithic die

UCIe™ Universal Chiplet Interconnect Express

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

UCIe-3D Approach: Towards Compelling KPIs

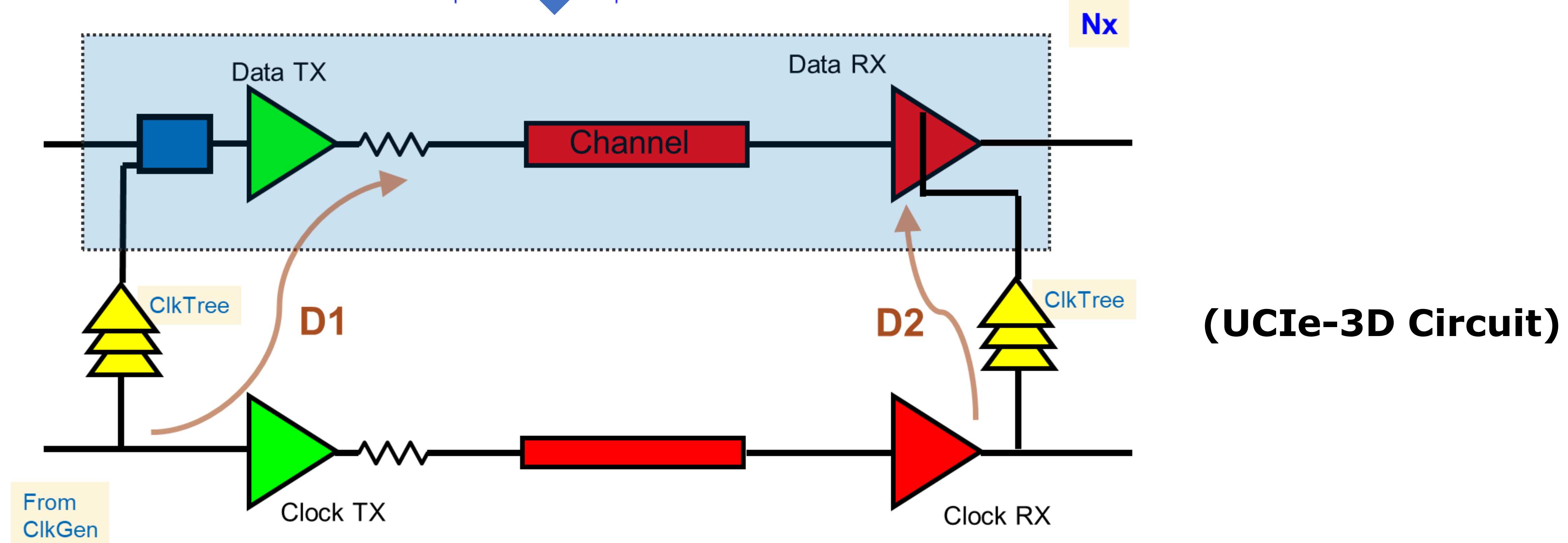
- PHY: unidirectional, forwarded clock, Hard IP
  - No ESD, inverter-based design
  - Lower frequency for lower power/area
  - No (de)serialization .. No deskew
- No D2D Adapter: NOC directly connected to PHY
  - BER 1E-27 -> 1E-30 – no CRC/ Replay
  - Repair: cluster level - a defect may impact multiple ubumps
- Centralized (chiplet) level function
  - Test, Debug, Pattern gen/ check Infrastructure (TDPI)
  - Amortizes overhead since there will be multiple Links



UCIe-3D: Significant Simplification over UCIe 2.5D/2D

Die-1
Die-2
NoC
D2D Adapter
Data
FIFO
Serializer
1-bit EQ
TXD
16x
/N
De-Skew
PLL
Clock
DLL
PI + DCC
CK Buf
TXCK
TXD
Phase Control
PHY
Data lane
T-line (UCIe-S)
RC wire (UCIe-A)
CLK Phase-1
CLK Phase-2
Track lane
De-Skew
RXD
Sampler/ Deserializer
FIFO
2/4 Phases
16x
Phase Gen
RXCK
RXD
Track Comp
PHY
Data
D2D Adapter
NoC
UCIe-S components

(UCIe 2D/2.5D Circuits)
(Note 2D / UCIe-S has more components)

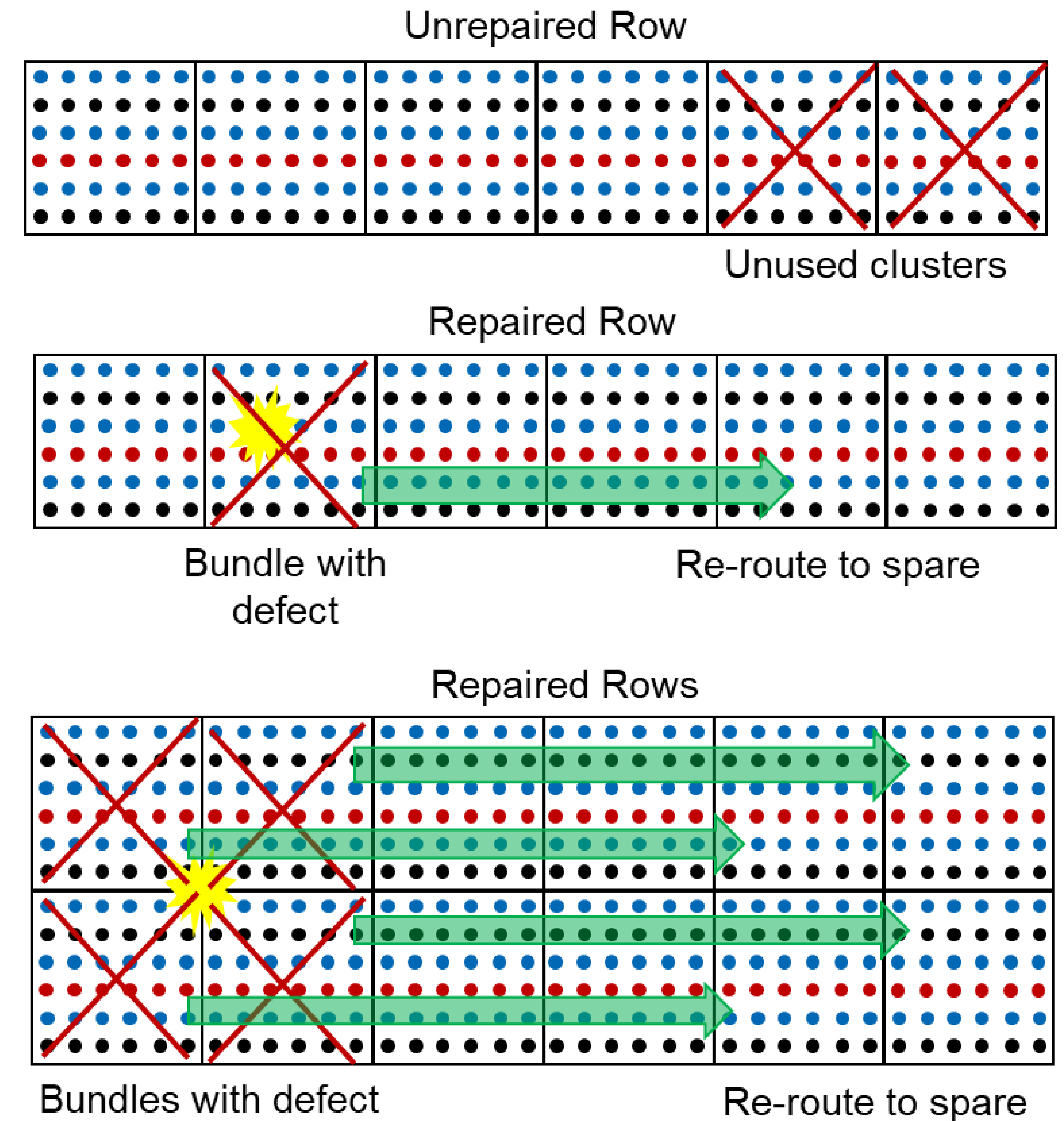


Universal Chiplet Interconnect Express

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

Repair: Baseline Approach

- Reserve modules in SoC for repair, reroute to the backup module when there is a failure.
  - To address cluster failure mode. Defects are larger than bumps. For example, one defect can take out 5x5 bump area.
- UCIe-3D: Each Module has one TX bundle (x64 TX + Clock) and one RX bundle (x64 RX + Clock). Bundle layout is roughly a square, ~ 100um x 100um for 9um bump pitch.
- For densely packed UCIe Module array, reserve 2 full Modules (4 bundles) to repair one failure cluster.
  - Assume alternating TX, RX bundle in at least one direction.



Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

Agenda

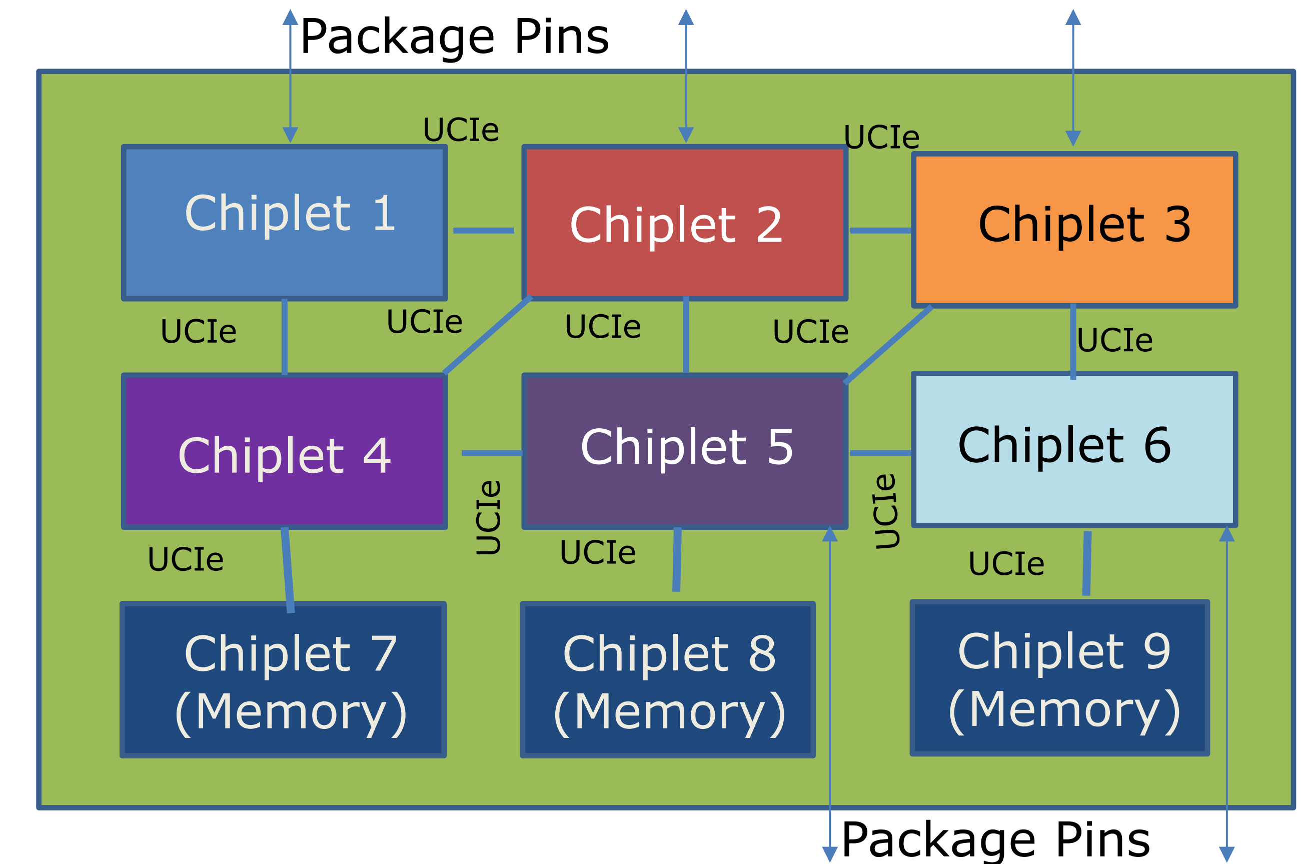
- Introducing UCIe
- UCIe 1.0/ UCIe 1.1 Specifications: Recap
- UCIe 2.0: Vertical Chiplets with UCIe-3D
- UCIe 2.0: Addressing SIP challenges through common infrastructure
- UCIe – Key Metrics
- Future Directions and Conclusions

UCIe™
Universal Chiplet Interconnect Express

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

SiP Challenges: Testability, Debug, Telemetry, and Manageability: Design for Testability/ Debug/ Manageability (DFx)

- UCIe 1.0/1.1 already has several mechanisms in place for DFx at the interconnect level
  - E.g., lane margin, loopback, compliance, fault reporting, sideband, etc
- Need to look at the entire chiplet/ package in a holistic manner to ensure a thriving chiplet-based plug-and-play ecosystem
- Test: Die / Sort, Package / Bond
  - Micro-bumps can not be probed => Use other bumps (e.g. JTAG, UCIe-S)
- Debug in lab and field (e.g., can not use a scope/ logic analyzer)
- Manageability w/ security (e.g., repair, firmware upgrades)
- Some chiplets may not have access to package pins
  - Use UCIe to access remote chiplets from chiplets with package pins (dedicated UCIe-S/ muxed)
- Wide range of bandwidth demands



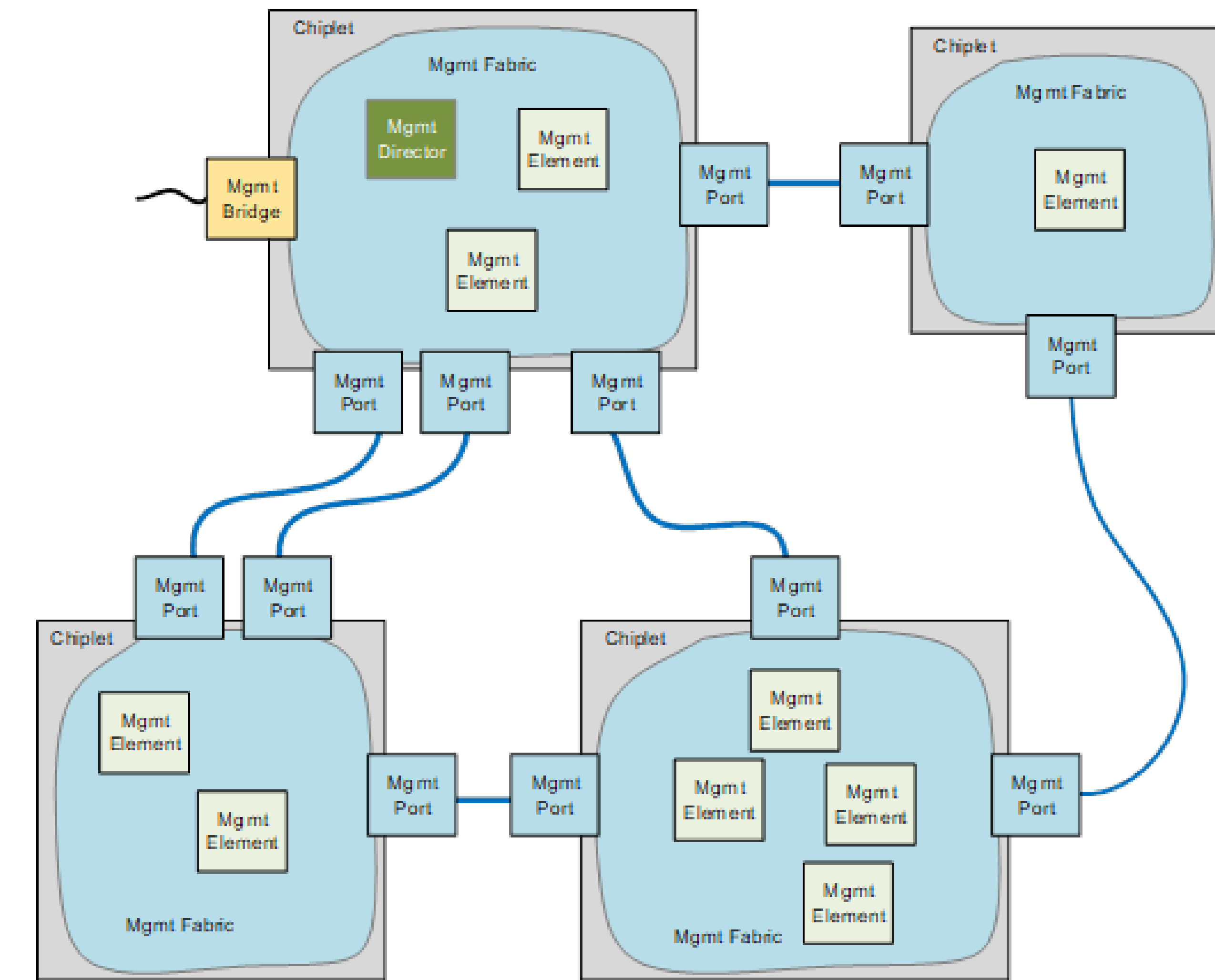
Interface	Bandwidth
UCIe-S x16	512 Gb/s/dir main @ 32G (800 Mb/s/dir sideband)
PCIe6.0 x16	1024 Gb/s/dir
USB 4.0	80 Gb/s/dir
JTAG (IEEE 1149.1)	5-100 Mb/s/dir
IEEE 1838	>100 Mb/s/dir with FPP
I2C/SMBus	400 Kb/s
I3C	33 Mb/s/dir

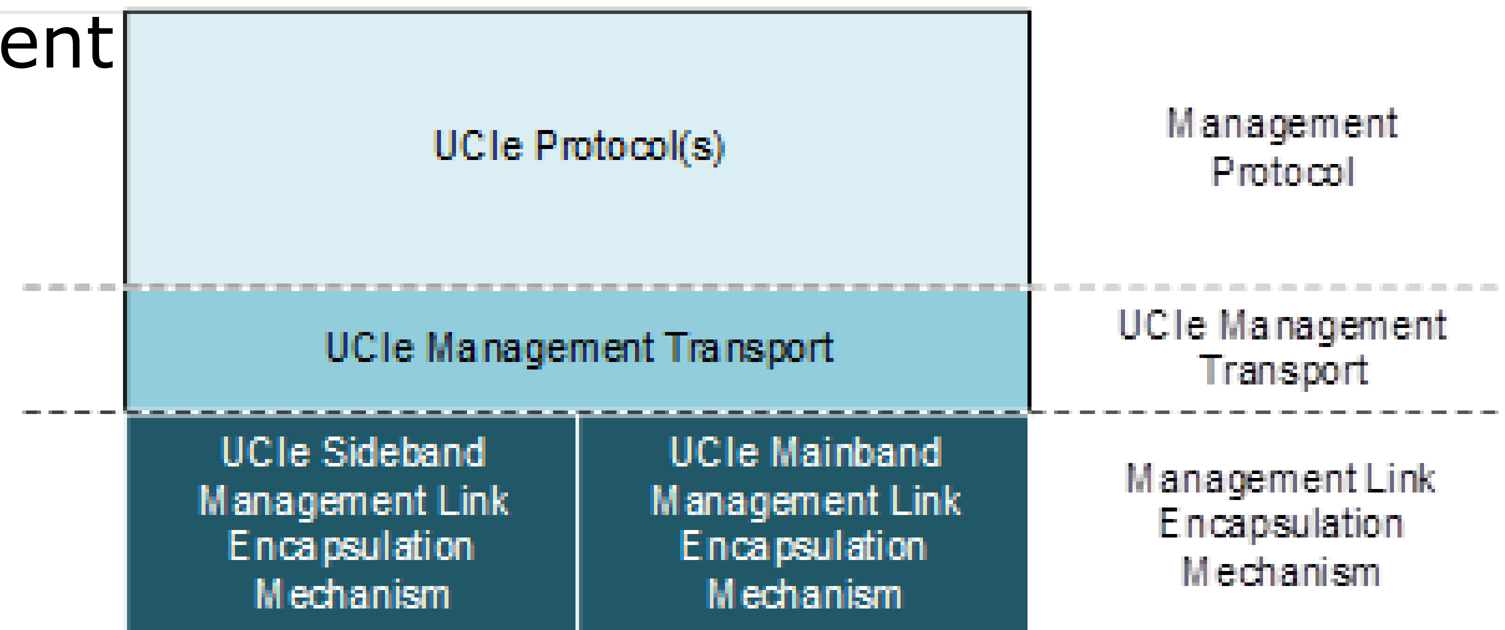
Common infrastructure for entire lifecycle.
Leverage existing package pins and standards
Added SB-only as well as x8 UCIe-S dedicated port for DFx

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

UCIe 2.0 Manageability Baseline Architecture

- Mechanisms supported: Discovery of chiplets and their configuration, initialization of chiplets and parameters (e.g., EEPROM replacement), firmware download, power/ thermal management, error reporting, telemetry, retrieval of crash dump log, test and debug, various aspects of chiplet security, etc.
- Protocol-agnostic – builds on top of existing industry standards
- Management domain: chiplets that support UCIe manageability are interconnected through management ports, with a bridge to an external package pin (e.g., SMBus, PCIe)
  - Chiplets that don't support UCIe management are outside the domain
  - Management director: discovery, configuration, coordination of overall management within SiP, root of trust for manageability
- UCIe Management Transport – end-to-end media-independent protocol for management communication on the management network (management entities within/ across chiplet(s))
- UCIe Management Transport Packet for communication
  - Sideband and Mainband
  - Up to 8 VCs, each with (un)ordered semantics
  - Credit based – negotiated during link training

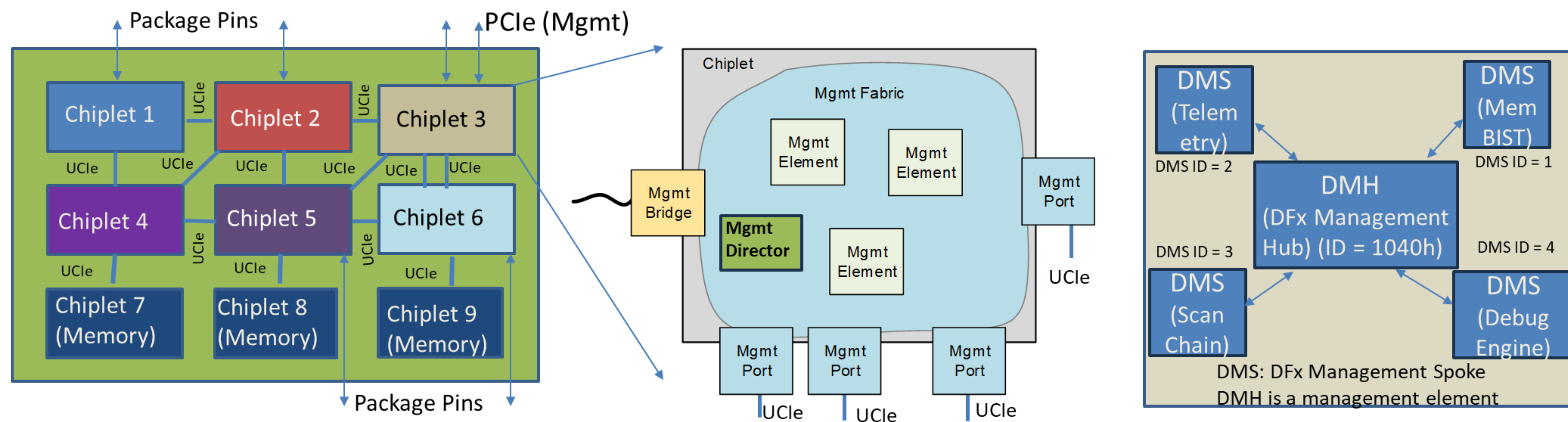




Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

UCIe DFx Architecture (UDA): Common Infrastructure

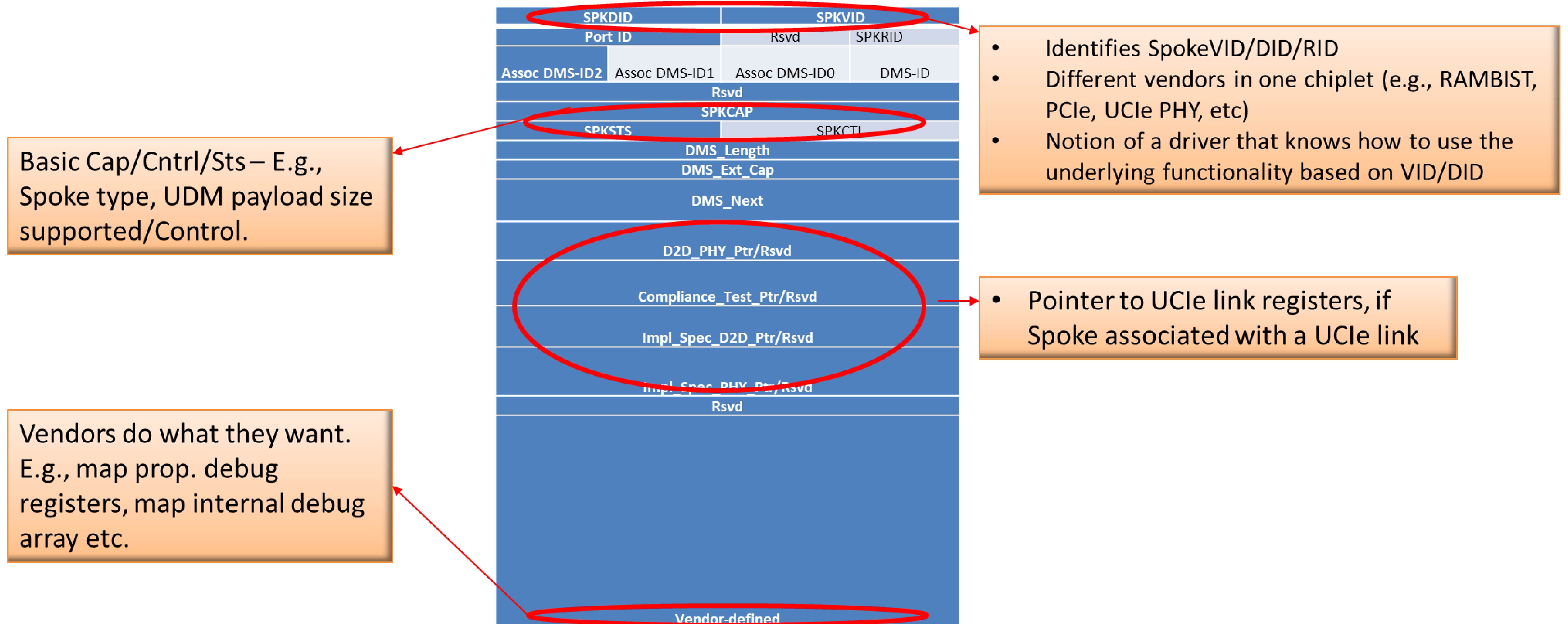
- UDA comprehends test, telemetry, debug – covered through the management fabric
- Hub and Spoke(s) inside each chiplet
- DFx Management Hub (DMH) is a management element
  - Gateway to access test, debug, telemetry capability inside each chiplet
  - Routes the management transport packets to Spokes (DFx Mgmt Spoke: DMS)
  - Routes to other chiplet (DMH)
- DMS: test, debug, telemetry functions
  - E.g., Scan controller, Mem BIST, SoC Fabric debug, trace protocol engine, etc.
- Architected configuration registers on top of existing registers – basically a UCIe wrapper on top of existing registers
- UCIe issued Vendor ID, Device ID , RID for spoke



UCIe Universal Chiplet Interconnect Express

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

Standardized Configuration for Test, Debug, Manageability

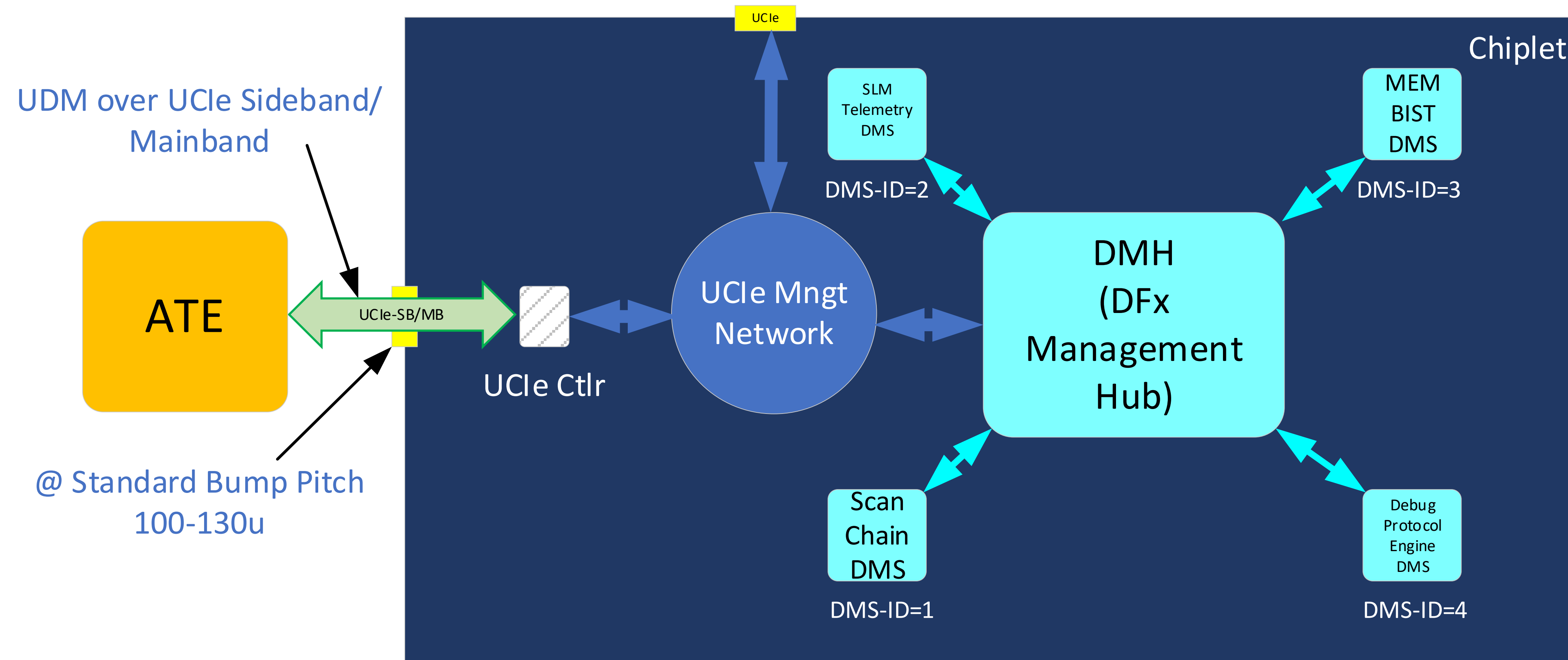


UDA: Simple, minimal standard header for DMS; rest is vendor-defined

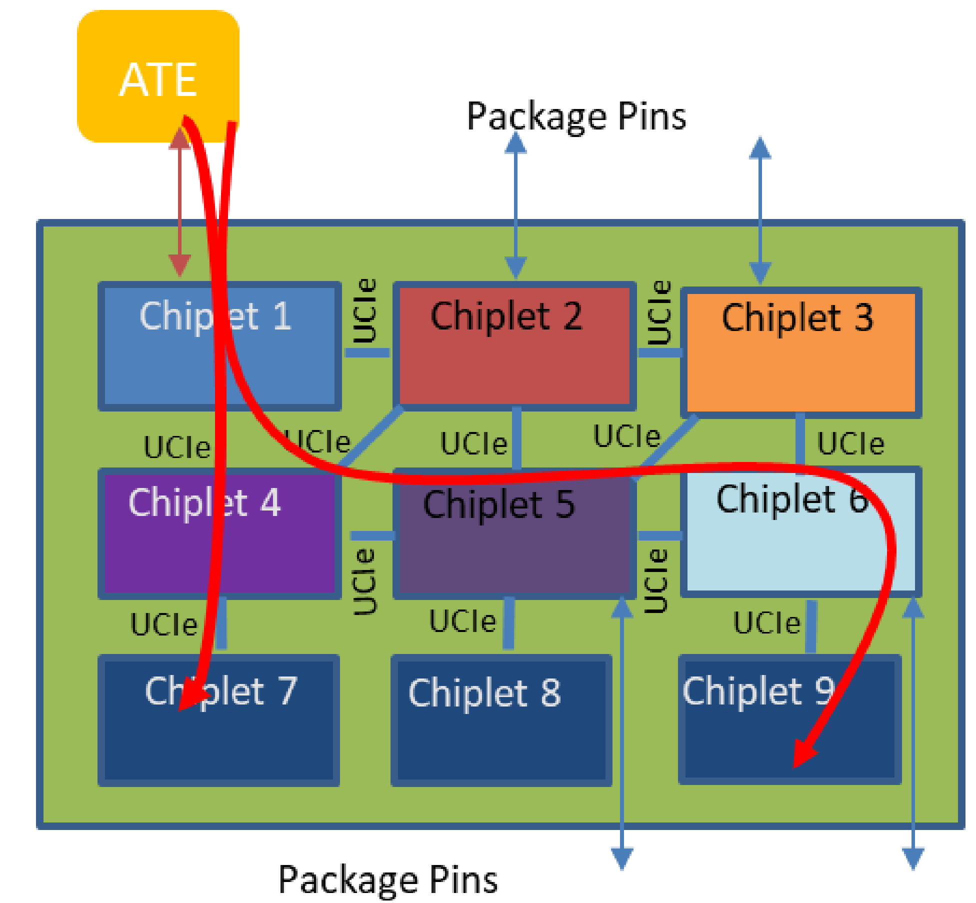
UCIe™ Universal Chiplet Interconnect Express

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

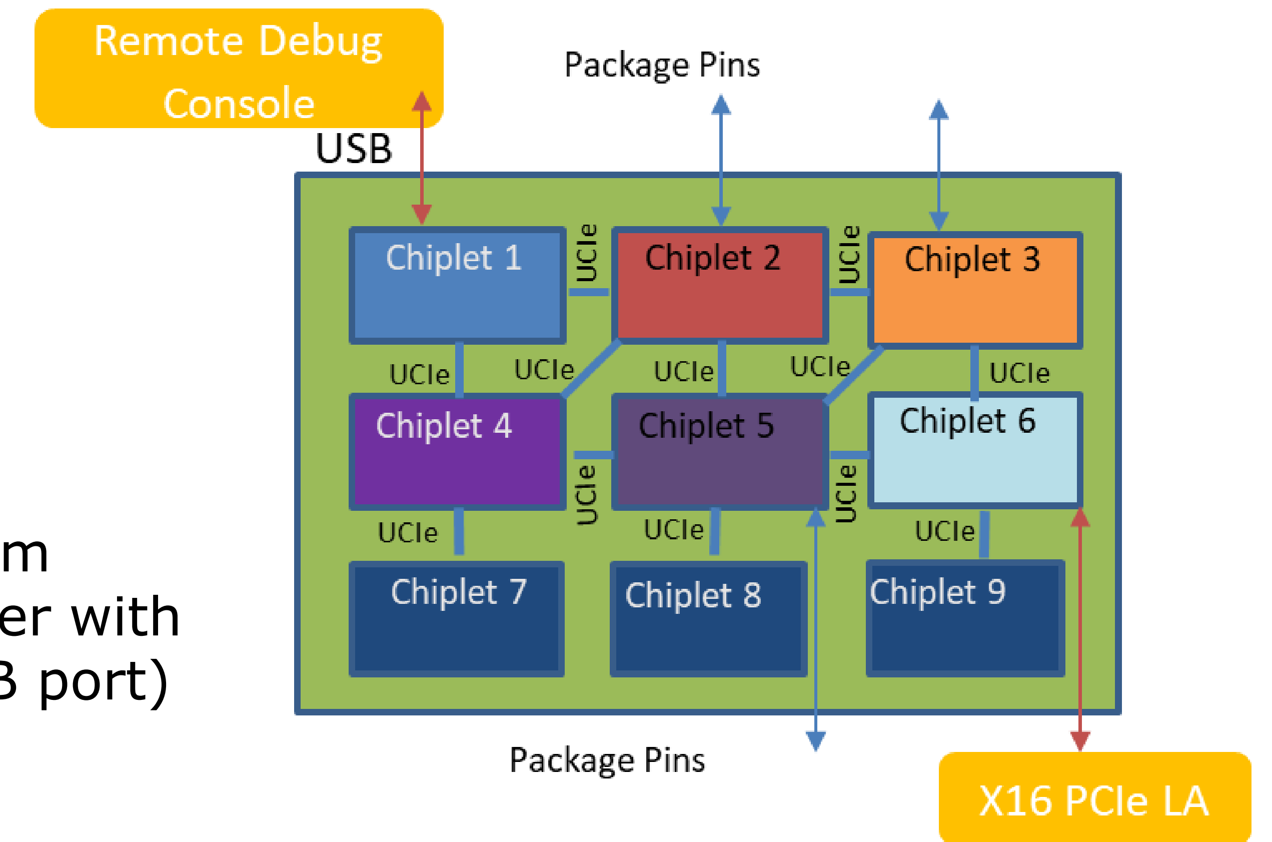
Example Usages of UDA



(a: ATE testing during sort using UCIe-S pins: sideband and/or mainband)



(b: ATE testing after packaging using UCIe-S pins: sideband/mainband)



Package pins used for Test & Debug

Package pins used for functional purposes

(c: Routing multiple sets of debug signals from Chiplets through UCIe to a PCIe Logic Analyzer with The remote debug console (control) on a USB port)

UCIe Universal Chiplet Interconnect Express

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

Key Metrics: Expanding Industry Leading KPIs to UCIe-3D

Characteristics / KPIs	UCIe-S (2D)	UCIe-A (2.5D)	UCIe 3D	Comments for UCIe 3D
Characteristics				
Data Rate (GT/s)	4, 8, 12, 16, 24, 32		Up to 4	= SoC Logic frequency – power efficiency is critical
Width (each cluster)	16	64	80	Options or reduced width to 70, 60…
Bump Pitch (μm)	100 – 130	25 – 55	≤ 10 (optimized) > 10 – 25 (functional)	Must scale so that UCIe-3D fits within the bump area, must support hybrid bonding
Channel Reach (mm)	≤ 25	≤ 2	3D vertical	FtF bonding initially; FtB, BtB, multi-stack possible
Target for Key Metrics				
BW Shoreline (GB/s/mm)	28 – 224	165 – 1317	N/A (vertical)	
BW Density (GB/s/mm^2)	22 – 125	188 – 1350	4,000 – 300,000	4TB/s/mm^2 @ 9μm, ~12TB/s/mm^2 @ 5μm, ~35TB/s/mm^2 @ 3μm, ~300TB/s/mm^2 @ 1 μm
Power Efficiency Target (pJ/b)	0.5	0.25	<0.05 at 9μm -> 0.01 at 1 μm	Conservatively estimated at 9μm pitch <0.02 for 3μm pitch
Low-Power Entry/Exit	0.5nS ≤ 16G, 0.5-1nS ≥ 24G		0nS	No preamble or post-amble
Reliability (FIT)	0 < FIT (Failure in Time) << 1		0 < FIT << 1	BER < 1E-27
ESD	30V CDM		5V CDM → ≤ 3V	5V CDM at introduction, no ESD for W2W hybrid bonding possible

UCIe-3D will deliver compelling power-efficient performance

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

Future Directions and Conclusions

- UCIe Consortium continues to evolve UCIe technology in a backward-compatible manner comprehending new usage models, additional cost optimization, and towards a robust compliance mechanism.
- UCIe is an open industry standard that establishes an open chiplet ecosystem and ubiquitous interconnect at the package level.
  - Tremendous support across the industry with several companies announcing IP/VIP availability
  - Evolving as *the* interconnect of SoCs just as PCIe and CXL at the board level
  - UCIe 2.0 Specification is available to the public https://www.uciexpress.org/specification
- UCIe Consortium welcomes interested companies and institutions to join the organization at the Contributor or Adopter level.
- 6 Technical Working Groups (Electrical, Protocol, Form Factor/Compliance, Manageability/Security, Systems and Software, Automotive) alongside the Marketing Working Group are driving the technology toward the future.
  - Incredible innovation happening in the Consortium!
- Get involved! Learn more by visiting www.UCIexpress.org

UCIe™
Universal Chiplet Interconnect Express

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

Questions?

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024

Thank You

www.UCIexpress.org

Property of Universal Chiplet Interconnect Express™ (UCIe ™) 2024