UCIe Consortium Releases 2.0 Specification
Supporting Manageability System Architecture and 3D Packaging

Key highlights:

- UCIe Consortium continues to advance an open chiplet ecosystem by releasing the latest specification supporting 3D packaging, manageability system architecture, and more.
- Specification update offers higher bandwidth density and improved power efficiencies.
- The UCIe 2.0 Specification is fully backward compatible and is now available to the public.

August 6, 2024 – Beaverton, OR – Today the Universal Chiplet Interconnect Express™ (UCIe™) Consortium announced the release of its 2.0 Specification. The UCIe 2.0 Specification adds support for a standardized system architecture for manageability and holistically addresses the design challenges for testability, manageability, and debug (DFx) for the SIP lifecycle across multiple chiplets – from sort to management in the field. The introduction of optional manageability features and a UCIe DFx Architecture (UDA), which includes a management fabric within each chiplet for testing, telemetry, and debug functions, allows vendor agnostic chiplet interoperability across a flexible and a unified approach to SIP management and DFx operations.

Additionally, the 2.0 Specification supports 3D packaging – offering higher bandwidth density and improved power efficiency compared to 2D and 2.5D architectures. UCIe-3D is optimized for hybrid bonding with a bump pitch functional for bump pitches as big as 10-25 microns to as small as 1 micron or less to provide flexibility and scalability.

Another feature is optimized package designs for interoperability and compliance testing. The goal of compliance testing is to validate the main-band supported features of a Device Under Test (DUT) against a known- good reference UCIe implementation. UCIe 2.0 establishes an initial framework for physical, adapter, and protocol compliance testing.

“UCIe Consortium is supporting a diverse range of chiplets to meet the needs of the rapidly changing semiconductor industry,” said Cheolmin Park, UCIe Consortium President and Corporate VP, Samsung Electronics. “The UCIe 2.0 Specification builds on previous iterations by developing a comprehensive solution stack and encouraging interoperability between chiplet solutions. This is yet another example of the Consortium’s dedication to the flourishing open chiplet ecosystem.”

Highlights of the UCIe 2.0 Specification:

- Holistic support for manageability, debug, and testing for any System-in-Package (SiP) construction with multiple chiplets.
- Support for 3D packaging to significantly enhance bandwidth density and power efficiency.
- Improved system-level solutions with manageability defined as part of the chiplet stack.
- Optimized package designs for interoperability and compliance testing.
- Fully backward compatible with UCIe 1.1 and UCIe 1.0.

The UCIe 2.0 Specification is available to the public by request at www.uciexpress.org/specifications.

Learn more about the UCIe 2.0 Specification at the Future of Memory and Storage (FMS)

Dr. Debendra Das Sharma, UCIe Consortium Chairman, will introduce new features included in the UCIe 2.0 Specification at FMS on Thursday, August 8, 2024, from 8:30 – 9:35 am PT in the Santa Clara Convention Center. UCIe Consortium will also host a kiosk in SNIA's Open Standards Pavilion on the exhibit show floor from August 6-8. Visit the FMS agenda for detailed information about UCIe Consortium's presentation and exhibit schedule: https://futurememorystorage.com/.

Resources:

- UCIe 2.0 Specification
- UCIe 2.0 White Paper
- UCIe Consortium member statement of support

About UCIe Consortium

The UCIe Consortium is an industry consortium dedicated to advancing UCIe™ (Universal Chiplet Interconnect Express™) technology, an open industry standard that defines the interconnect between chiplets within a package, enabling an open chiplet ecosystem and ubiquitous interconnect at the package level. UCIe Consortium is led by key industry leaders Advanced Semiconductor Engineering, Inc. (ASE), Alibaba, AMD, Arm, Google Cloud, Intel Corporation, Meta, Microsoft Corporation, NVIDIA, Qualcomm Incorporated, Samsung Electronics, and Taiwan Semiconductor Manufacturing Company, and represents more than 130 member companies. For more information, visit www.UCIexpress.org.

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