Statement of Support for the UCIe 2.0 Specification

Advantest Corporation
"As a manufacturer of automated test equipment (ATE), Advantest joined the UCIe consortium to ensure the testability of individual chiplets and complex multi-die devices. As a result, the latest UCIe spec now includes an optional, dedicated test access port (TAP) utilizing UCIe-S channels for high-bandwidth production test access. We strongly believe that the industry needs such a standardized TAP and will continue to work with EDA vendors, foundries, and partners to enable the UCIe ecosystem."
Juergen Serrer, CTO, Advantest Corporation

Alphawave Semi
"As chiplets increasingly gain adoption in hyperscalers, high-performance computing (HPC) and artificial intelligence (AI) systems, the heterogeneous approach demands diverse requirements tailored to a variety of applications. Alphawave Semi is dedicated to enhancing its UCIe IP subsystem and chiplets according to the latest available UCIe standards. The UCIe 2.0 specification marks a significant advancement with the introduction of UCIe-3D over hybrid bonding. Alphawave Semi aims to streamline its portfolio with the latest updates from the UCIe 2.0 specification and to collaborate closely with customers and ecosystem partners to enable chiplet connectivity solutions."
Mohit Gupta, Senior VP & GM, Custom Silicon & IP, Alphawave Semi

AMD
"Enabling core density is a critical component of achieving, both, increased performance and energy efficiency for processors across consumer and commercial applications. The UCIe 2.0 specification introduces support for advanced 3D packaging technologies that enable higher compute and bandwidth density in modern CPUs, GPUs and Accelerators. We are extremely proud to collaborate with our industry peers in the UCIe Consortium in order to support a robust vendor-neutral chiplet ecosystem."
Anwar Kashem, Corporate Vice President, IO Architecture, AMD

Arm
"Arm is at the center of the industry's leading multi-vendor chiplet ecosystem, delivering platforms and Compute Subsystems that maximize efficiency without compromising performance or driving up costs. Aligning our standardization efforts to UCIe 2.0 exemplifies the kind of innovation that can be unlocked through industry collaboration, such as providing partners with a path to 3D packaging support to enable advanced system designs with higher bandwidth, lower latency, and significant cost savings."
Andy Rose, VP Technology Strategy and Fellow, Arm

Astera Labs
“Chiplets are a critical component to enable increased scalability, performance, and flexibility for accelerated computing platforms in AI infrastructure. The UCIe 2.0 Specification is a significant milestone for the chiplet ecosystem as it delivers improvements to both overall performance and interoperability. Astera Labs is proud to continue supporting this important initiative, which offers an expanded range of solutions for our Intelligent Connectivity Platform to address an increasingly diverse set of AI platforms with faster deployment cycles.”
Casey Morrison, Chief Product Officer, Astera Labs

Ayar Labs
“The UCIe 2.0 specification is critical for the interconnect chiplet ecosystem and sets the stage for unleashing next-gen AI architectures. Ayar Labs is at the forefront of this movement, centering our TeraPHY™ optical I/O chiplet roadmap around the UCIe specification. The UCIe Consortium’s work is instrumental in driving broad adoption and manufacturability of optical I/O to deliver the high bandwidth, energy efficiency, and low latency required for AI innovation and application growth.”
Lakshmikant (LK) Bhupathi, Vice President of Products, Strategy and Ecosystem, Ayar Labs

Blue Cheetah
"The enthusiasm for chiplets has never been higher, and the evolution of the UCIe specification underscores that interest. Continued advancement in customizable die-to-die interconnects is critical to enabling multi-vendor chiplet ecosystems and products."
Elad Alon, CEO, Blue Cheetah

Cadence
"Cadence has a strong history of working closely with the UCIe Consortium to contribute to and develop the UCIe standard. The changes in UCIe 2.0, particularly enhanced interoperability through management mechanisms and the introduction of the UCIe-3D solution, enable many more chiplet designers and SiP implementers to use UCIe to achieve faster time to market while lowering design costs. These are the right steps toward making UCIe a truly universal standard for chiplet interconnect that supports a thriving open chiplet ecosystem. Cadence is pleased to bring these innovations to our users."
Boyd Phelps, Senior Vice President and General Manager of the Silicon Solutions Group, Cadence

Eliyan
“Eliyan congratulates the UCIe Consortium on the UCIe 2.0 release, and is pleased to contribute our expertise to the progress of the UCIe specification, including authoring one of the ECNs in the 2.0 release. Eliyan developed a 32Gbps UCIe PHY in standard packaging last year, and recently developed a beyond 32Gbps+ UCIe PHY in advanced packaging. Eliyan will continue to offer a range of the highest performance and lowest power PHYs for standards-compliant and customized die-to-die solutions.”
Farhad Tabrizi, Vice President of Standards & Alliances, Eliyan

eTopus
“UCIe Spec Ver 1.1 established the foundation of a die-to-die specification that achieves high-bandwidth density, low latency, and high power-efficiency. With UCIe 2.0, additional requirements for support blocks such as the reference clock are now clearly defined. The Management Transport Protocol establishes a framework beyond die-to-die data transfer toward System-in-Package management support of data and control between die utilizing this higher layer UCIe protocol. This will enable our customers to architect more efficient SiP solutions with debug and test support. We applaud the work of the UCIe Consortium and member companies and are pleased to be active contributors to this important work.”
Harry Chan, CEO, eTopus

Global UniChip Corporation (GUC)
"In two years since its announcement UCIe became an enabler of chiplet-based large-scale AI, HPC and Networking products. UCIe-2.0 specification is the next step in implementing a vision of interoperable chiplets using the full spectrum of standard and advanced 2.5D and 3D packaging technologies. GUC, an advanced packaging expert, was an early UCIe adopter and has a rich portfolio of interface IPs with UCIe-2.0 compliant 32Gbps IP, which will be silicon proven in Q1/2025, as well as 64Gbps IP, currently in development. GUC was the earliest implementer of 3DIC technology with 3D interface IP supporting UCIe-3D specification silicon proven at 5.0Gbps using TSMC’s SoIC-X."
Igor Elkanovich, CTO, GUC

Google
“Google is pleased to see the progress that UCIe has made over the past two years to bring the industry together to deliver an open, interoperable and multi-vendor chiplet ecosystem. UCIe 2.0 delivers three major features to advance the state of the art. The management protocol provides the foundation for serviceability and reliability, while the standard debug and test architecture fosters compliance to a common criteria amongst different vendors. Finally, Google is excited to see UCIe introduce 3D capabilities to advance in-package IO technology for HPC and AI applications.”
Partha Ranganathan, Fellow and Vice President, Google

Intel
“To realize the full potential of AI, we need an open and collaborative ecosystem that fosters advanced packaging and chip design innovation across market segments. Today marks another milestone of progress with the UCIe 2.0 specification, which helps us push the boundaries of what’s possible and address what customers are asking for – AI compute solutions that deliver power-efficient performance.”
Justin Hotard, Executive Vice President and General Manager of the Data Center and Artificial Intelligence Group, Intel

Kandou
"Kandou is proud to be a Contributor member of the UCIe Consortium. As a pioneer in chiplet technology, we believe strong partnerships and collaboration are key to establishing interoperability and furthering the advancement of the industry. The release of the UCIe 2.0 specification shows that we are closer to achieving these interoperable solutions across multiple applications."
Dr. Amin Shokrollahi, CEO & Founder, Kandou

Mercedes-Benz
"Mercedes-Benz is thrilled about the ongoing progress of UCIe and the advancements in the UCIe 2.0 specification. Enhancements like 3D packaging promise higher bandwidth density and improved power efficiency, while optimized package designs ensure interoperability and compliance testing. With the Automotive Working Group addressing key automotive and safety requirements, Mercedes-Benz proudly supports the UCIe Consortium's efforts. We look forward to continuing our contribution to the standardization of the chiplet ecosystem."
Georges Massing, Vice President MB.OS Automated Driving & E/E Integration, Mercedes-Benz

Microchip
"UCIe 2.0 enables a broad industry die-to-die interconnect ecosystem which allows for high function integration which we anticipate will add a great deal of value to Microchip's industry-leading portfolio of compute and systems solutions. The new features in this open standard, enabling multi-die solutions, are optimized for performance, power and cost efficiency."
Pete Hazen, Vice President, Data Center Solutions Business Unit, Microchip

MIPS Technology
"MIPS Technology is very pleased with the UCIe 2.0 specification, which enhances high-performance, cost-effective multi-chip solutions. Building on the robust features of UCIe 1.1, UCIe 2.0 improves debug capabilities, test methodologies, and packaging technologies, ensuring greater efficiency and reliability in advanced applications, including AI/ML use cases."
Durgesh Srivastava, CTO, MIPS Technology

Neuron IP
"Neuron IP is proud to be at the forefront of silicon interfaces with the development of UCIe. The need for 'standardized' chiplet interfaces is paramount to the evolution of silicon industry and is an integral part to all rapidly-advancing application verticals including AI/ML, HPC/Data Center, 5G/6G, and Automotive. In the upcoming 2.0 Specification, UCIe extends to 3D IC packaging; paving the way for cutting-edge logic die stacking. We are excited to enable incredibly dense, power-efficient systems-in-package."
Saman Sadr, President & CEO, Neuron IP

NVIDIA
"The release of the UCIe 2.0 Specification marks a significant milestone in the evolution of chiplet-based system design, offering a standardized way of initializing, managing, and debugging systems-on-a-chip. As a member of the UCIe Consortium, NVIDIA is committed to advancing all aspects of this specification to help drive innovation and performance in next-generation computing systems."
Ashish Karandikar, Vice President of Hardware Engineering, NVIDIA

Rebellions
“Rebellions is excited to support the UCIe 2.0 Specification, which promises significant advancements in chiplet-based AI accelerators. Already utilizing UCIe v1.1, Rebellions remains dedicated to expanding the chiplet ecosystem and will actively leverage and develop chiplet-based architectures in collaboration with various vendors across UCIe layers. UCIe 2.0's new features, including its manageability architecture and Debug and Test Architecture (UDA), will enhance our time-to-market and cost-effectiveness. This enables Rebellions to deliver cutting-edge AI accelerators with superior interoperability, performance, and security as we scale out our AI core chiplet developments.”
Jinwook Oh, CTO, Rebellions

Samsung Electronics
"Chiplets have become an essential solution for all applications ranging from AI to automotive. As one of the founding members of the UCIe Consortium, we are delighted to participate in the successful release of the UCIe 2.0 specification. Samsung Foundry is actively building the UCIe ecosystem with multiple partners through our Multi-Die Integration (MDI) Alliance, and we anticipate UCIe 2.0 to expand our chiplet-based solution offerings, and add more value to Samsung Foundry's turnkey services."
Jongshin Shin, Corporate Executive Vice President of Foundry IP Development, Samsung Electronics

Siemens EDA
“Building on our leadership in chiplets technology and strong track record of support for the standard, Siemens EDA is once again a key contributor for the newest version of UCIe technology. With our UCIe 2.0 Verification IP and Compliance Test Suite solutions, Siemens continues its UCIe design verification leadership. And because version 2.0 of the UCIe standard incorporates advances that support mainstream design for test (DFT) practices, it paves the way for next-generation products capable of fully leveraging Siemens’ industry-leading Tessent software.”
Mike Ellow, CEO of Silicon Systems, Siemens EDA

Synopsys
“The latest advancements in the UCIe 2.0 specification accelerate the industry’s adoption of 3D packaging for power efficiency and higher bandwidth density, while also addressing the complexities in testing and debug across the silicon lifecycle. As an active contributor to the UCIe Consortium, Synopsys is helping to drive the development and adoption of the UCIe standard for fast heterogeneous integration of chiplets with industry-leading, comprehensive UCIe IP and multi-die solutions.”
Michael Posner, Vice President of IP Product Management, Synopsys

UniVista
“As a contributor of the UCIe Consortium and its working groups, Univista is proud to integrate our UCIe 1.1 IP subsystem into customer’s design rapidly. The consortium has released UCIe 1.1 which shows short latency, high bandwidth density and power efficiency, and enabled multiple companies to adopt UCIe as Die-to-Die interface in their design. The newly released UCIe 2.0 introduces UCIe-3D, which provides interface specifications for 3D homogeneous and heterogeneous design. Univista will continue the IP development of new version UCIe.”
Mao Liu, Vice President, UniVista

Untether AI
“Untether AI is excited to incorporate the UCIe 2.0 specification in our designs, enabling energy-efficient and seamless communication for our high-performance AI acceleration chiplets. This integration supports our groundbreaking at-memory compute architecture, enhancing our ability to deliver compact and high-performance systems for datacenter, automotive, and other key application.”
Chris Walker, CEO, Untether AI